

HIGH PERFORMANCE DIFFERENTIAL OSCILLATOR SERIES „DLPO-3“ 1.0—220 MHz

FEATURES

- + 100% pin-to-pin drop-in replacement to quartz and MEMS based XO
- + Differential Oscillator for Low Cost
- + Extremely low RMS phase jitter of 0.6ps
- + Low power consumption
- + Excellent long time reliability
- + Very tight frequency stability as low as ± 10 ppm possible
- + Outstanding long term aging
- + LVPECL and LVDS output signals
- + Standard housings: 3.2x2.5; 5.0x3.2; 7.0x5.0 mm
- + Pb-free, RoHS and REACH compliant / MSL1@260°C

APPLICATIONS

- + 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI Express,
- + Telecom, networking, instrumentation, storage, servers
- + etc.

GENERAL DATA

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LVPECL AND LVDS, COMMON ELECTRICAL CHARACTERISTICS						
Supply Voltage	V _{DD}	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
		2.25	-	3.63	V	Termination schemes in Figures 1 and 2 - XX ordering code
		1.71	1.8	1.89	V	Only for LVDS output
Output Frequency Range	f	1	-	220	MHz	
Frequency Stability	F _{stab}	-10	-	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
		-20	-	+20	PPM	
		-25	-	+25	PPM	
		-50	-	+50	PPM	
First Year Aging	F _{aging1}	-2	-	+2	PPM	25°C
10-year Aging	F _{aging10}	-5	-	+5	PPM	25°C
Operating Temperature Range	T _{use}	-40	-	+85	°C	Industrial
		-20	-	+70	°C	Extended Commercial
Input Voltage High	V _{IH}	70%	-	-	V _{DD}	Pin 1, OE or ST
Input Voltage Low	V _{IL}	-	-	30%	V _{DD}	Pin 1, OE or ST
Input Pull-up Impedance	Z _{in}	-	100	250	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	-	-	MΩ	Pin 1, ST logic low
Start-up Time	T _{start}	-	6	10	ms	Measured from the time V _{DD} reaches its rated minimum value.
Resume Time	T _{resume}	-	6	10	ms	In Standby mode, measured from the time ST pin crosses 50% threshold.
Duty Cycle	DC	45	-	55	%	Contact PETERMANN-TECHNIK for tighter duty cycle

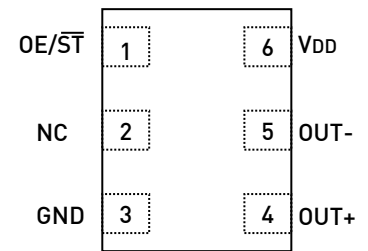
GENERAL DATA (continued)

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LVPECL, DC AND AC CHARACTERISTICS						
Current Consumption	I _{DD}	–	61	69	mA	Excluding Load Termination Current, V _{DD} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	35	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	–	1	µA	OE = Low
Standby Current	I _{std}	–	–	100	µA	ST = Low, for all V _{DDs}
Maximum Output Current	I _{driver}	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	V _{OH}	V _{DD} -1.1	–	V _{DD} -0.7	V	See Figure 1(a)
Output Low Voltage	V _{OL}	V _{DD} -1.9	–	V _{DD} -1.5	V	See Figure 1(a)
Output Differential Voltage Swing	V _{Swing}	1.2	1.6	2.0	V	See Figure 1(b)
Rise/Fall Time	T _r , T _f	–	300	700	ps	20% to 80%, see Figure 1(a)
OE Enable/Disable Time	T _{oe}	–	–	115	ns	f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Period Jitter	T _{jitt}	–	1.2	1.7	ps	f = 100 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, V _{DD} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{DDs}
LVDS, DC AND AC CHARACTERISTICS						
Current Consumption	I _{DD}	–	47	55	mA	Excluding Load Termination Current, V _{DD} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	35	mA	OE = Low
Differential Output Voltage	V _{OD}	250	350	450	mV	See Figure 2
Output Disable Leakage Current	I _{leak}	–	–	1	µA	OE = Low
Standby Current	I _{std}	–	–	100	µA	ST = Low, for all V _{DDs}
V _{OD} Magnitude Change	ΔV _{OD}	–	–	50	mV	See Figure 2
Offset Voltage	V _{OS}	1.125	1.2	1.375	V	See Figure 2
V _{OS} Magnitude Change	ΔV _{OS}	–	–	50	mV	See Figure 2
Rise/Fall Time	T _r , T _f	–	495	700	ps	20% to 80%, see Figure 2
OE Enable/Disable Time	T _{oe}	–	–	115	ns	f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Period Jitter	T _{jitt}	–	1.2	1.7	ps	f = 100 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, V _{DD} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{DDs}
EXCELLENT RELIABILITY DATA						
MTBF						500 million hours
Shock Resistance:						10.000 g
Vibration Resistance:						70 g

PIN DESCRIPTION

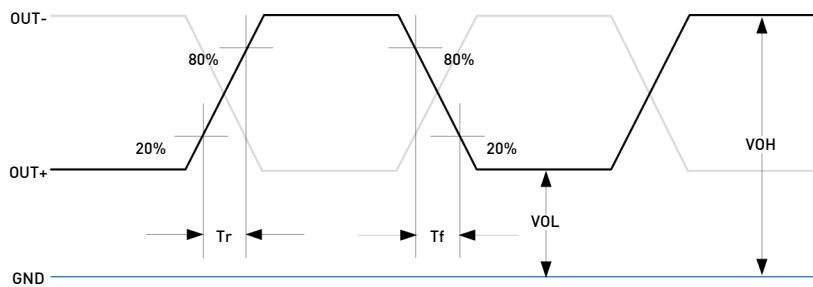
PIN	SYMBOL	FUNCTIONALITY
1	OE	Input H or Open: specified frequency output L: output is high impedance
	ST	Input H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_std.
2	NC	NA No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power VDD Power Supply Ground
4	OUT+	Output Oscillator output
5	OUT-	Output Complementary oscillator output
6	VDD	Power Power Supply Voltage

TOP VIEW



WAVE FORM DIAGRAMS

FIGURE 1(A). LVPECL VOLTAGE LEVELS PER DIFFERENTIAL PIN (OUT+/OUT-)



WAVE FORM DIAGRAMS (continued)

FIGURE 1(B). LVPECL VOLTAGE LEVELS ACROSS DIFFERENTIAL PAIR

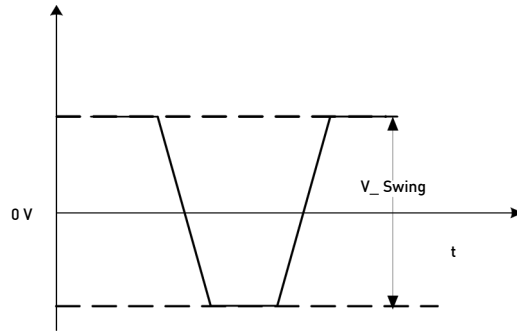
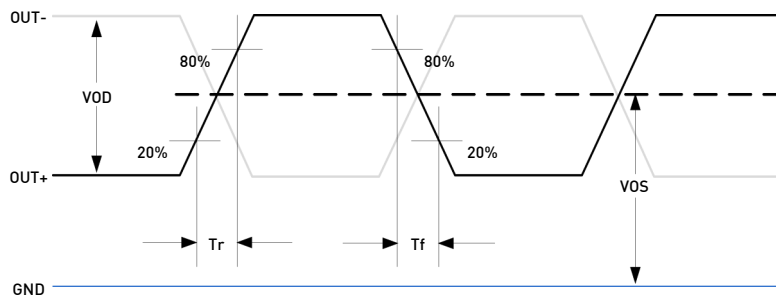


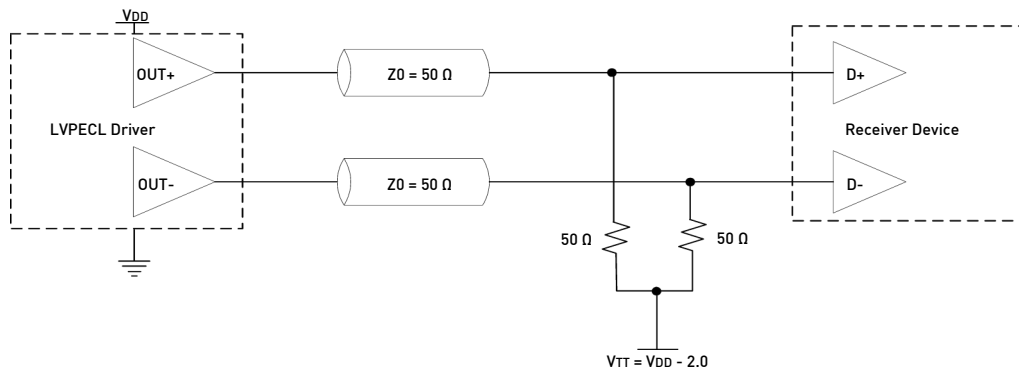
FIGURE 2. LVDS VOLTAGE LEVELS PER DIFFERENTIAL PIN (OUT+/OUT-)



TERMINATION DIAGRAMS

LVPECL:

FIGURE 3. LVPECL TYPICAL TERMINATION



TERMINATION DIAGRAMS (continued)

LVPECL:

FIGURE 4. LVPECL AC COUPLED TERMINATION

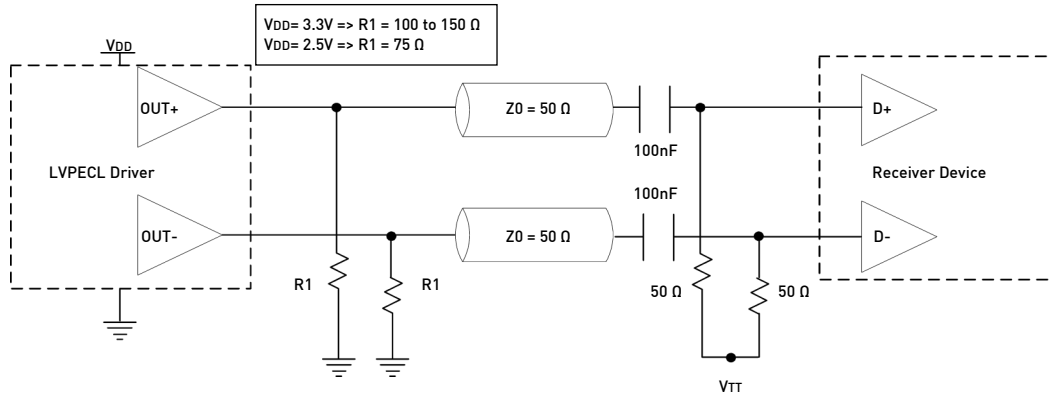
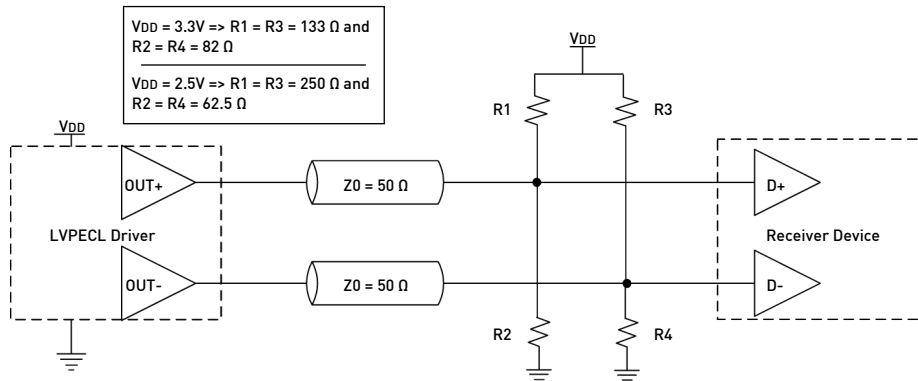


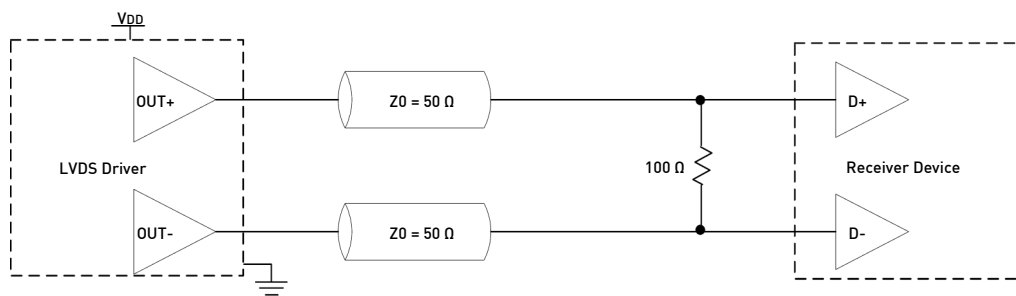
FIGURE 5. LVPECL WITH THEVENIN TYPICAL TERMINATION



TERMINATION DIAGRAMS

LVDS:

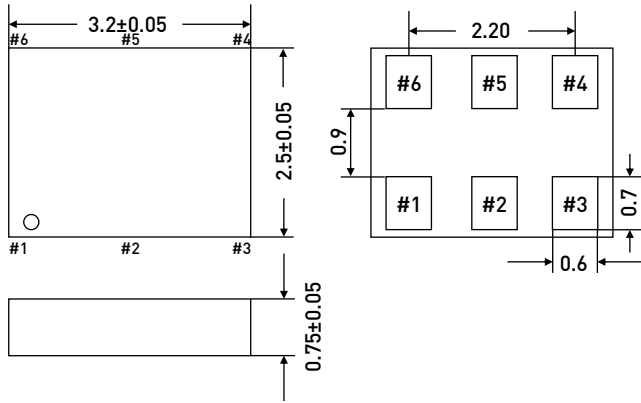
FIGURE 6. LVDS SINGLE TERMINATION (LOAD TERMINATED)



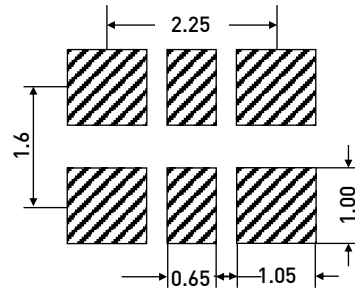
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

3.2X 2.5 X 0.75 MM

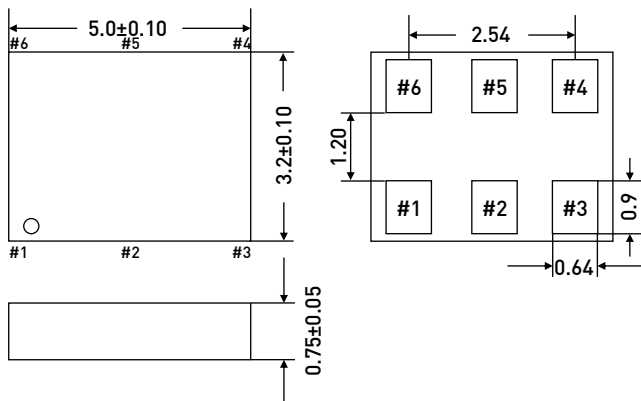


RECOMMENDED LAND PATTERN (UNIT:MM)^[1]

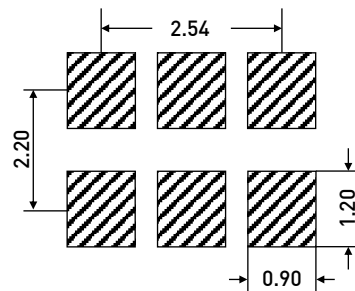


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

5.0X 3.2 X 0.75 MM

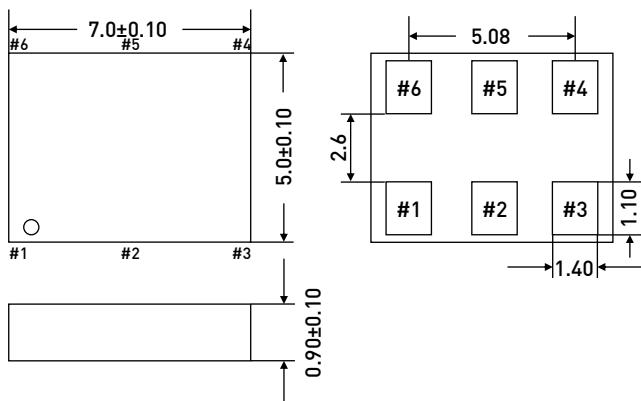


RECOMMENDED LAND PATTERN (UNIT:MM)^[1]

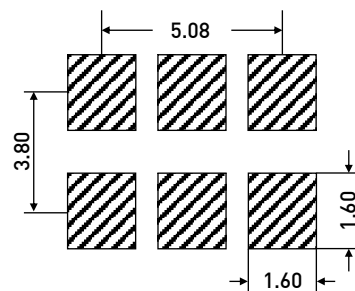


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

7.0X 5.0 X 0.90 MM



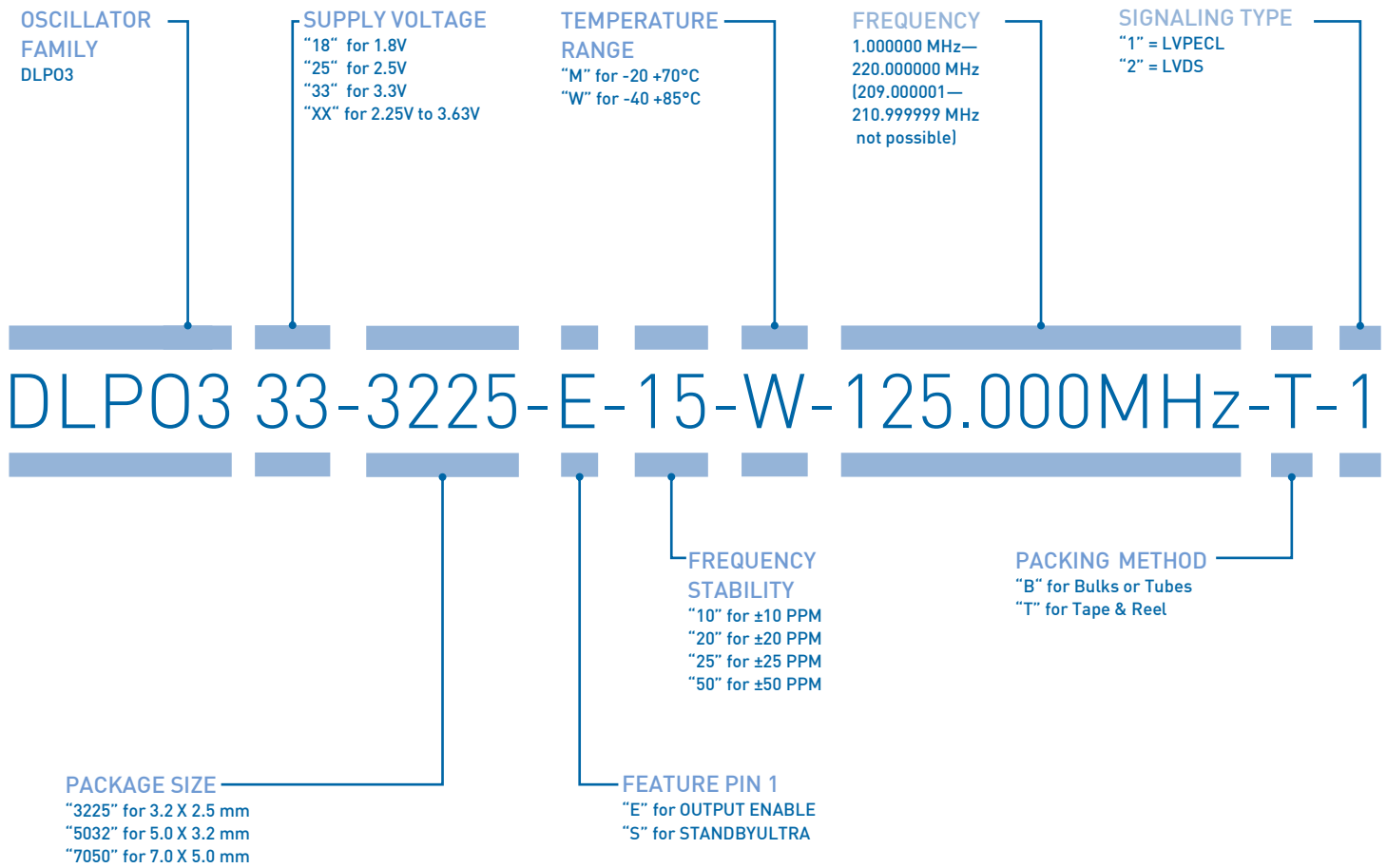
RECOMMENDED LAND PATTERN (UNIT:MM)^[1]



Note:

1. A capacitor value of 0.1 μ F between VDD and GND is recommended.

ORDERING INFORMATION

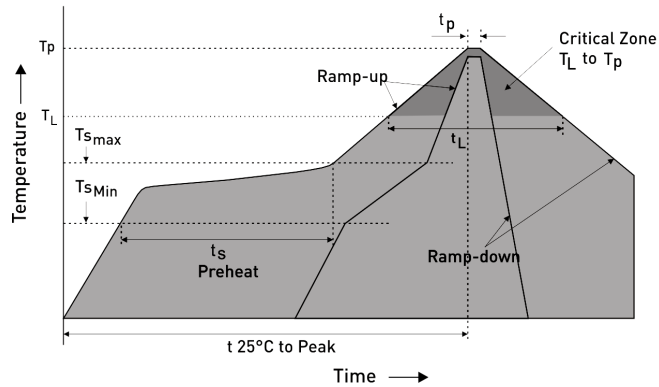


EXAMPLE: DLPO333-3225-E-15-W-125.000MHz-T-1

[PLEASE CLICK HERE TO CREATE YOUR OWN ORDERING CODE](#)

SAMPLES ARE AVAILABLE WITHIN A SHORT DELIVERY PERIOD!

REFLOW SOLDER PROFILE



IPC/JEDEC Standard	IPC/JEDEC J-STD-020
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Typical (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum
Target Peak Temperature (TP Target)	255°C
Time within 5°C of actual peak (tP)	20 - 40 Seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

PREMIUM QUALITY BY PETERMANN-TECHNIK



OUR COMPANY IS CERTIFIED ACCORDING TO ISO 9001:2015 IN OCTOBER 2016 BY THE DMSZ CERTIFIKATION GMBH.

THIS IS FOR YOU TO ENSURE THAT THE PRINCIPLES OF QUALITY MANAGEMENT ARE FULLY IMPLEMENTED IN OUR QUALITY MANAGEMENT SYSTEM AND QUALITY CONTROL METHODS ALSO DOMINATE OUR QUALITY STANDARDS.

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