

HIGH TEMPERATURE LOW POWER OSCILLATOR

SERIES „HTLPO“ 115—137 MHz

FEATURES

- + 100% pin-to-pin drop-in replacement to quartz MEMS based XO
- + High Temperature Low Power Oscillator for Low Cost
- + Excellent long time reliability—outperforms quartz-based XO
- + Operating temperature from -40°C to 125°C / -55°C to 125°C optional
- + Supply voltage of 1.8V, 2.5V to 3.3V
- + Excellent total frequency stability as low as ± 20 ppm
- + LVCMOS/LVTTL compatible output
- + Express samples within 1 day ex works PETERMANN-TECHNIK
- + Pb-free, RoHS and REACH compliant / MSL1@260°C

APPLICATIONS

All applications within -40/+125°C (non AEC-Q100 automotive and avionics)

GENERAL DATA^[1,2]

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
FREQUENCY RANGE						
Output Frequency Range	f	115.2	–	137	MHz	
FREQUENCY STABILITY AND AGING						
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance at 25°C, 1st year aging at 25°C,
		-25	–	+25	PPM	and variations over operating temperature, rated power
		-30	–	+30	PPM	supply voltage and load (15 pF ± 10%).
		-50	–	+50	PPM	
OPERATING TEMPERATURE RANGE						
Operating Temperature Range	T_use	-40	–	+105	°C	
		-40	–	+125	°C	
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
SUPPLY VOLTAGE AND CURRENT CONSUMPTION						
Supply Voltage	V _{DD}	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	I _{DD}	–	6.2	8	mA	No load condition, f = 125 MHz, V _{DD} = 2.8V, 3.0V, or 3.3V
		–	5.4	7	mA	No load condition, f = 125 MHz, V _{DD} = 2.5V
		–	4.8	6	mA	No load condition, f = 125 MHz, V _{DD} = 1.8V
OE Disable Current	I _{OD}	–	–	4.5	mA	V _{DD} = 2.5V to 3.3V, OE = Low, output in high Z state
		–	–	4.0	mA	V _{DD} = 1.8V, OE = Low, output in high Z state
Standby Current	I _{std}	–	2.6	8.5	μA	V _{DD} = 2.8V to 3.3V, ST = Low, output is pulled down
		–	1.4	5.5	μA	V _{DD} = 2.5V, ST = Low, output is pulled down
		–	0.6	3.5	μA	V _{DD} = 1.8V, ST = Low, output is pulled down

Note: 1. All electrical specifications in the above table are specified with 15 pF output load at default drive strength and for all VDD(s) unless otherwise stated.
2. The typical value of any parameter in the Electrical Characteristic table is specified for the nominal value of the highest voltage option for that parameter and at 25 °C temperature.

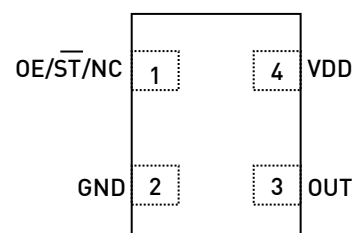
GENERAL DATA (continued)

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LVCMOS OUTPUT CHARACTERISTICS						
Duty Cycle	DC	45	–	55	%	All V _{DD} s
Rise/Fall Time	T _r , T _f	–	1.0	2.0	ns	V _{DD} = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	V _{DD} = 1.8V, 20% - 80%
		–	1.0	3.0	ns	V _{DD} = 2.25V - 3.63V, 20% - 80%
Output High Voltage	V _{OH}	90%	–	–	V _{DD}	I _{OH} = -4 mA (V _{DD} = 3.0V or 3.3V) I _{OH} = -3 mA (V _{DD} = 2.8V and V _{DD} = 2.5V) I _{OH} = -2 mA (V _{DD} = 1.8V)
Output Low Voltage	V _{OL}	–	–	10%	V _{DD}	I _{OL} = 4 mA (V _{DD} = 3.0V or 3.3V) I _{OL} = 3 mA (V _{DD} = 2.8V and V _{DD} = 2.5V) I _{OL} = 2 mA (V _{DD} = 1.8V)
INPUT CHARACTERISTICS						
Input High Voltage	V _{IH}	70%	–	–	V _{DD}	Pin 1, OE or ST
Input Low Voltage	V _{IL}	–	–	30%	V _{DD}	Pin 1, OE or ST
Input Pull-up Impedance	Z _{in}	50	87	150	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	–	–	MΩ	Pin 1, ST logic low
STARTUP AND RESUME TIMING						
Startup Time	T _{start}	–	–	5	ms	Measured from the time V _{DD} reaches its rated minimum value
Enable/Disable Time	T _{oe}	–	–	130	ns	f = 115.2MHz. For other frequencies, T _{oe} = 100 ns + 3* clock periods
Resume Time	T _{resume}	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
JITTER						
RMS Period Jitter	T _{jitt}	–	1.6	2.5	ps	f = 125 MHz, V _{DD} = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.8	3	ps	f = 125 MHz, V _{DD} = 1.8V
Peak-to-peak Period Jitter	T _{pk}	–	12	20	ps	f = 125 MHz, V _{DD} = 2.5V, 2.8V, 3.0V or 3.3V
		–	14	30	ps	f = 125 MHz, V _{DD} = 1.8V
RMS Phase Jitter (random)	T _{phj}	–	0.5	0.9	ps	f = 125 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	f = 125 MHz, Integration bandwidth = 12 kHz to 20 MHz
EXCELLENT RELIABILITY DATA						
MTBF						500 million hours
Shock Resistance:						10.000 G
Vibration Resistance:						70 g

PIN DESCRIPTION

PIN	SYMBOL	FUNCTIONALITY
1	OE/ ST/ NC	Output Enable H ^[3] : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby H ^[3] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I _{std} .
		No connect Any voltage between 0 and V _{DD} or Open ^[3] . Specified frequency output. Pin 1 has no function.
2	GND	Power Electrical ground ^[4]
3	OUT	Output Oscillator output
4	V _{DD}	Power Power supply voltage ^[4]

TOP VIEW



Note: 3. In OE or ST mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
4. A capacitor value of 0.1 μF between V_{DD} and GND is recommended.

TEST CIRCUIT DIAGRAMS FOR LVCMOS AND CLIPPED SINEWAVE OUTPUTS

FIGURE 1. TEST CIRCUIT

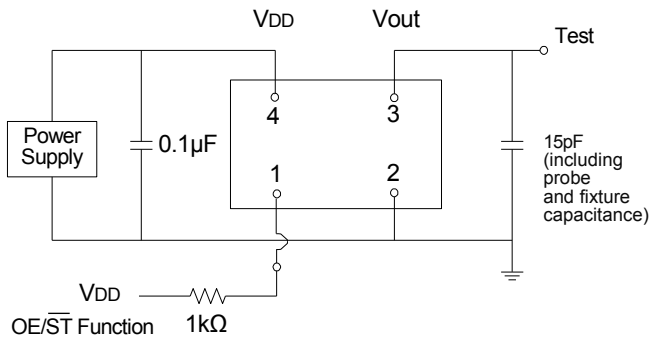
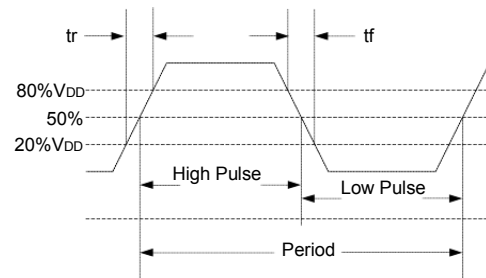


FIGURE 2. WAVEFORM



TIMING DIAGRAMS

FIGURE 3. STARTUP TIMING (OE/ST MODE)

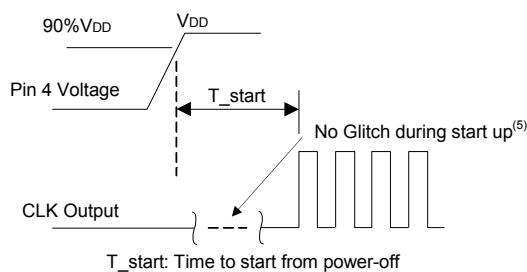


FIGURE 4. STANDBY RESUME TIMING (ST MODE ONLY)

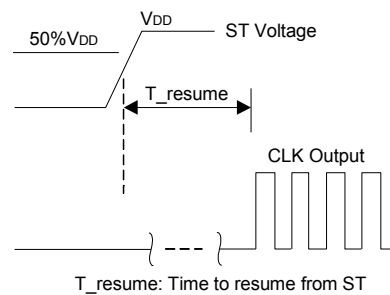


FIGURE 5. OE ENABLE TIMING (OE MODE ONLY)

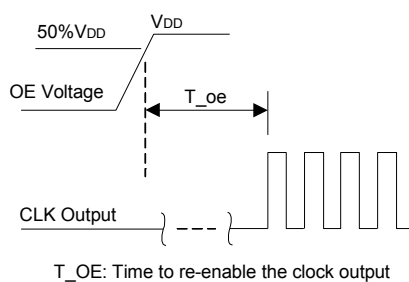
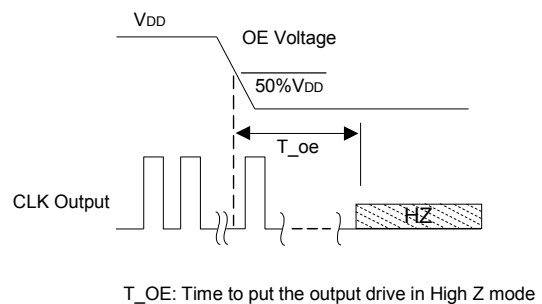


FIGURE 6. OE DISABLE TIMING (OE MODE ONLY)



Note: 5. HTLPO has "no runt" pulses and "no glitch" output during startup or resume.

PROGRAMMABLE DRIVE STRENGTH

The HTLPO includes a programmable drive strength feature named SoftLevel to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

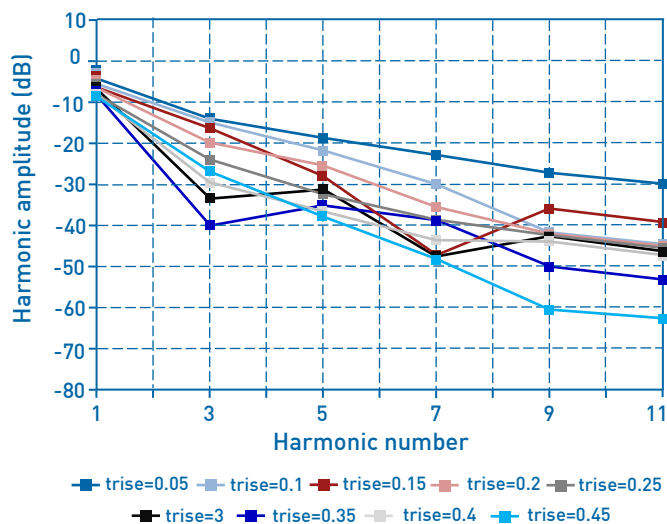
- + Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- + Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- + Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the Petermann-Technik Applications Note section: <http://www.petermann-technik.com>

EMI REDUCTION BY SLOWING RISE/FALL TIME (SoftLevel FUNCTION)

Figure 7 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

FIGURE 7. HARMONIC EMI REDUCTION AS A FUNCTION OF SLOWER RISE/FALL TIME (SoftLevel FUNCTION)



JITTER REDUCTION WITH FASTER RISE/FALL TIME

Power supply noise can be a source of jitter for the downstream chip-set. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The HTLPO provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

HIGH OUTPUT LOAD CAPABILITY

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V HTLPO device with default drive strength setting, the typical rise/fall time is 0.46ns for 5 pF output load. The typical rise/fall time slows down to 1ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the drive strength setting on the HTLPO to "F".

The HTLPO can support up to 30 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Fall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

HTLPO DRIVE STRENGTH SELECTION

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the HTLPO nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

CALCULATING MAXIMUM FREQUENCY

Based on the rise and fall time data given in Tables 1 through 5, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max. frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

where Trf_{20/80} is the typical value for 20%-80% rise/fall time.

EXAMPLE 1

Calculate f_{MAX} for the following condition:

- + VDD = 3.3V (Table 5)
- + Capacitive Load: 30pF
- + Desired Tr/f time = 1.46 ns (rise/fall time part number code=U)

Part number for the above example:

HTLP033-2520-E-25-Y-125.000MHz-T-S

Drive strength code is inserted here. Standard setting is "S"

RISE/FALL TIME (20% TO 80%) vs C_{LOAD}

TABLE 1. VDD = 1.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF
T	0.93	n/a ⁽⁶⁾	n/a
E	0.78	n/a	n/a
U	0.70	1.48	n/a
S for standard	0.65	1.30	n/a

TABLE 2. VDD = 2.5V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF
R	1.45	n/a	n/a
B	1.09	n/a	n/a
T	0.62	1.28	n/a
E	0.54	1.00	n/a
S for standard	0.43	0.96	n/a
F	0.34	0.88	n/a

TABLE 3. VDD = 2.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T	0.55	1.12	n/a
E	0.44	1.00	n/a
S for standard	0.34	0.88	n/a
F	0.29	0.81	1.48

TABLE 4. VDD = 3.0V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
S for standard	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

TABLE 5. VDD = 3.3V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
S for standard	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

Note: 6. "n/a" in Table 1 to Table 5 indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.

PROGRAMMABLE DRIVE STRENGTH

PIN 1 CONFIGURATION OPTIONS (OE, ST, OR NC)

Pin 1 of the HTLPO can be programmed to support three modes: Output enable (OE), standby (ST) or No Connect (NC).

OUTPUT ENABLE (OE) MODE

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

STANDBY (ST) MODE

In the ST mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few µA. When ST is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

NO CONNECT (NC) MODE

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1. Table 6 below summarizes the key relevant parameters in the operation of the device in OE, ST, or NC mode.

TABLE 6. OE vs. ST vs. NC

	OE	ST	NC
Active current 125 MHz (max, 1.8V)	6 mA	6 mA	6 mA
OE disable current (max. 1.8V)	4 mA	N/A	N/A
Standby current (typical 1.8V)	N/A	0.6 uA	N/A
OE enable time at 125 MHz (max)	130 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	pull-down	N/A

OUTPUT ON STARTUP AND RESUME

The HTLPO comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the HTLPO has NO RUNT, NO GLITCH output during startup or resume as shown in the waveform captures in Figure 8 and Figure 9.

FIGURE 8. STARTUP WAVEFORM vs. VDD

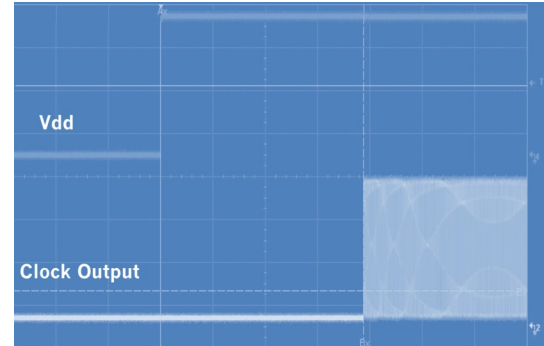
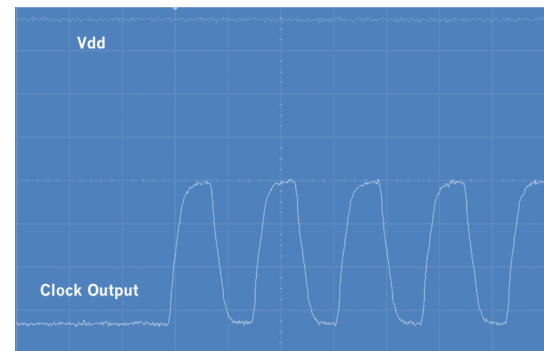


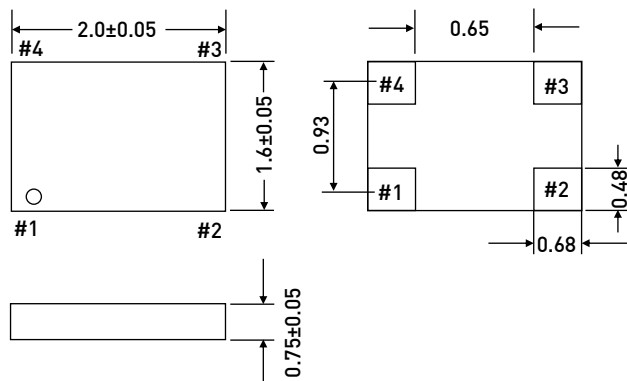
FIGURE 9. STARTUP WAVEFORM vs. VDD (ZOOMED-IN VIEW OF FIGURE 8)



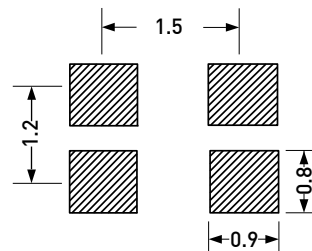
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.0 X 1.6 X 0.75 MM

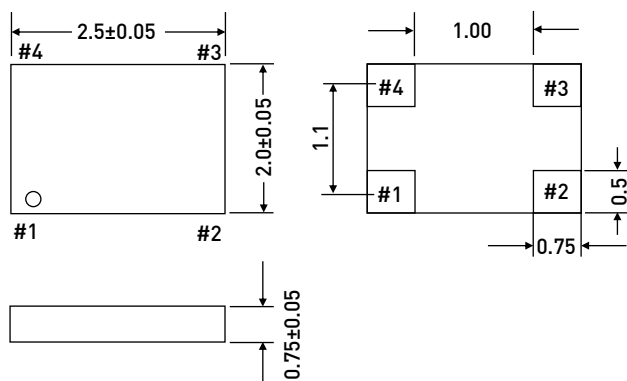


RECOMMENDED LAND PATTERN (UNIT:MM) [7]

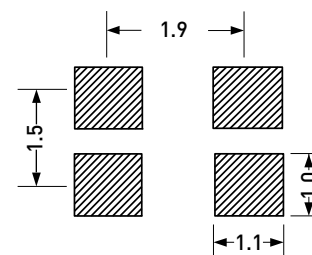


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.5 X 2.0 X 0.75 MM

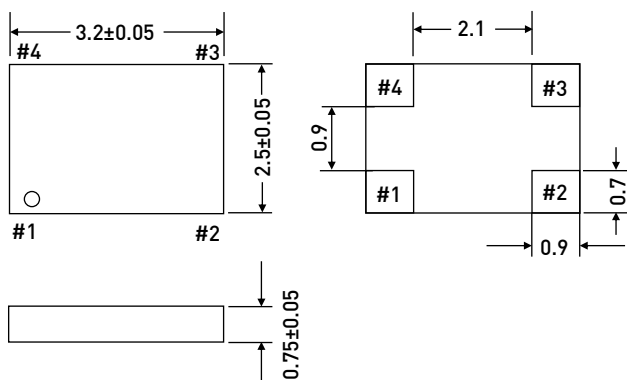


RECOMMENDED LAND PATTERN (UNIT:MM)

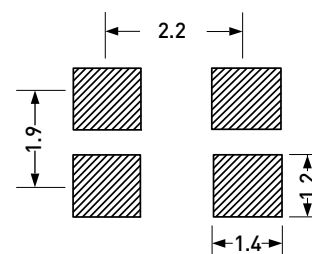


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

3.2 X 2.5 X 0.75 MM



RECOMMENDED LAND PATTERN (UNIT:MM)

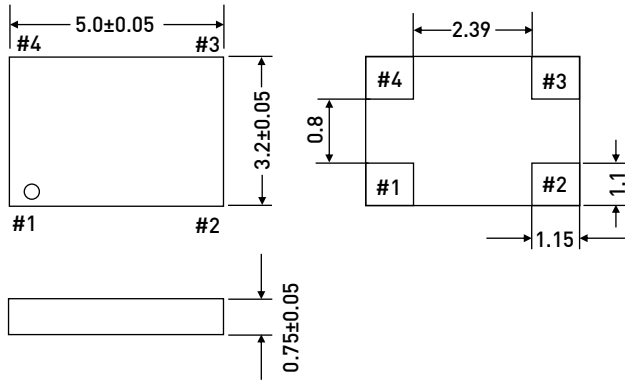


Note: 7. A capacitor value of 0.1 μ F between VDD and GND is recommended.

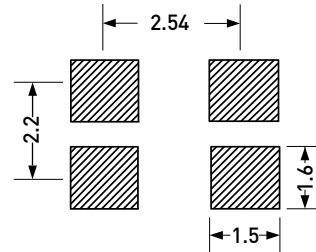
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

5.0 X 3.2 X 0.75 MM

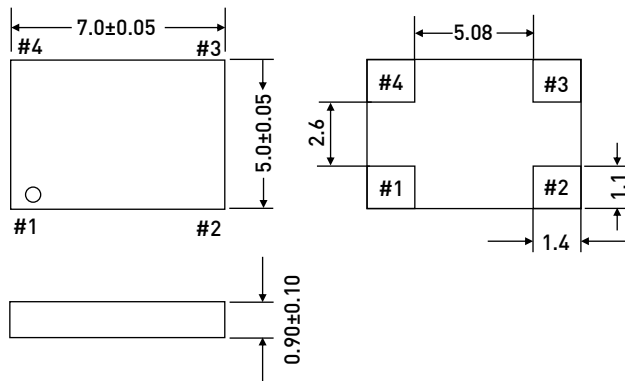


RECOMMENDED LAND PATTERN (UNIT:MM) [8]

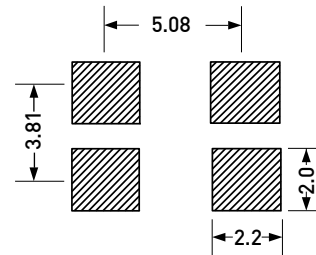


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

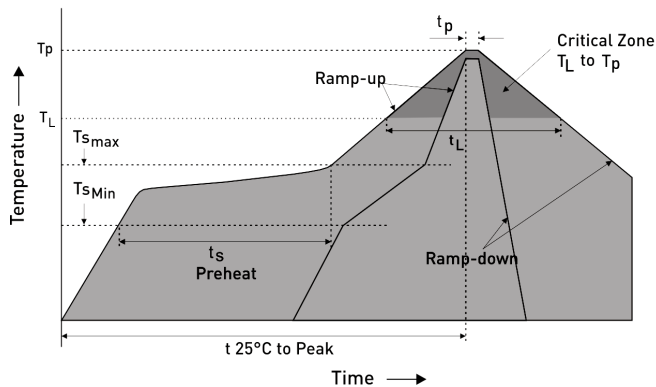
7.0 X 5.0 X 0.90 MM



RECOMMENDED LAND PATTERN (UNIT:MM)



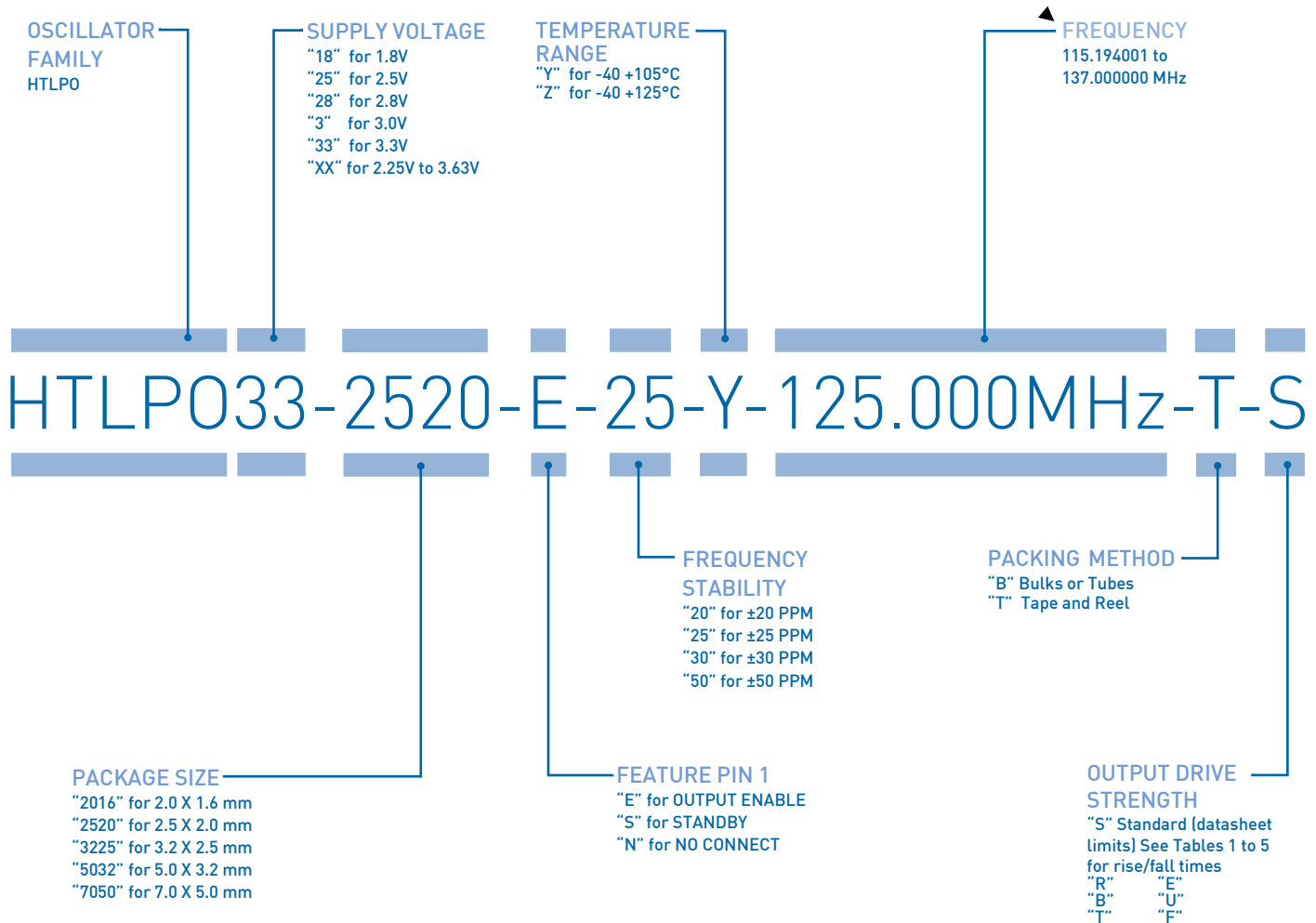
REFLOW SOLDER PROFILE



IPC/JEDEC Standard	IPC/JEDEC J-STD-020
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Typical (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum
Target Peak Temperature (TP Target)	255°C
Time within 5°C of actual peak (tP)	20 - 40 Seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

Note: 8. A capacitor value of 0.1 µF between VDD and GND is recommended.

ORDERING INFORMATION



EXAMPLE: HTLP033-2520-E-25-Y-125.000MHz-T-S

[PLEASE CLICK HERE TO CREATE YOUR OWN ORDERING CODE](#)

SAMPLES ARE AVAILABLE WITHIN A SHORT DELIVERY PERIOD!



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