PETERMANN TECHNIK
your clocking experts

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ULTRA-LOW POWER HIGH PRECISION OSCILLATOR

SERIES „ULPPO“ 32.768 kHz

FEATURES

+ Ultra Low Power High Precision Oscillator for Low Cost
+ Excellent long time reliability—outperforms quartz-based XO
+ 32.768 kHz ±5, ±10, ±20 ppm frequency stability options
+ World's smallest high precision 32.768 kHz Oscillator in a 1.5 x 0.8 mm housing
+ Ultra-low power: <1 µA
+ V_{DD} supply range: 1.5V to 3.63V
+ Improved stability reduces system power
+ Internal filtering eliminates external V_{DD} bypass cap and saves space
+ Programmable output swing for lowest power
+ Pb-free, RoHS and REACH compliant / MSL1@260°

APPLICATIONS

+ Smart Phones
+ Tablets
+ Health and Wellness Monitors
+ Fitness Watches
+ Sport Video Cams
+ Wireless Keypads
+ Ultra-Small Notebook PC
+ Pulse-per-Second (pps) Timekeeping
+ RTC Reference Clock
+ Battery Management Timekeeping
+ Wearables
+ IoT
+ GPS
+ Smart Metering
+ Home Automation

GENERAL DATA

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
FREQUENCY						
Output Frequency	F_out		32.768		kHz	
FREQUENCY STABILITY						
Frequency Stability Over Temperature[1] (without Initial Offset[2])	F_stab	-5.0		+5.0	PPM	Stability part number code = 5A
		-10		+10	PPM	Stability part number code = 10B
		-20		+20	PPM	Stability part number code = 20X
Frequency Stability Over Temperature (with Initial Offset[2])	F_stab	-10		+10	PPM	Stability part number code = 5A
		-13		+13	PPM	Stability part number code = 10B
		-22		+22	PPM	Stability part number code = 20X
Frequency Stability vs Voltage	F_V_{DD}	-0.75		+0.75	PPM	1.8V ±10%
		-1.5		+1.5	PPM	1.5V –3.63V%
First Year Frequency Aging	F_aging	-1.0		+1.0	PPM	TA = 25°C V_{DD} = 1.8 to 3.3V
10-year Aging	F_aging		1.5		PPM	TA = 25°C V_{DD} = 1.8 to 3.3V
20-year Aging	F_aging		2.0		PPM	TA = 25°C V_{DD} = 1.8 to 3.3V
OPERATING TEMPERATURE RANGE						
Operating Temperature Range	T_use	0	–	+70	°C	Commercial
		-40	–	+85	°C	Industrial
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
SUPPLY VOLTAGE AND CURRENT CONSUMPTION						
Operating Supply Voltage	V_{DD}	1.5		3.63	V	TA = -40°C to +85°C
Core Supply Current [3]	I_{DD}		0.99		µA	TA = 25°C, V_{DD} = 1.8V, LVCMOS Output configuration, No Load
	I_{DD}			1.52	µA	TA = -40°C to +85°C, V_{DD} =1.5V –3.63V, No load
Power-Supply Ramp	t_V_{DD}_Ramp			100	ms	V_{DD} Ramp-up 0 to 90% V_{DD}, TA = -40°C to +85°C
Start-up Time at Power-up	t_start		180	300	ms	TA= -40°C +60°C, valid output
	t_start			350	ms	TA = +60°C to +70°C, valid output
	t_start			380	ms	TA = +70°C to 85°C, valid output

Notes: 1.No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled, Calculating Load Current.

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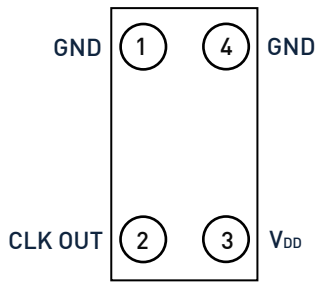
GENERAL DATA (continued)

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
JITTER PERFORMANCE (TA = OVER TEMP)						
Long Term Jitter				2.5	ps_{pp}	81920 cycles (2.5 sec), 100 samples
Period Jitter			35		ns_{RMS}	Cycles = 10,000, TA = 25°C, V_{DD} = 1.5V – 3.63V
LVCMOS OUTPUT (STANDARD VERSION)						
Output Rise/Fall Time	tf, tf		100	200	ns	10-90% (V_{DD}), 15 pF Load
Output Rise/Fall Time	tf, tf			50	ns	10-90% (V_{DD}), 5 pF Load, V_{DD} ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	V_{DD}: 1.5V – 3.63V. IOH = -1µA, 15 pF Load
Output Voltage Low	VOL			10%	V	V_{DD}: 1.5V – 3.63V. IOL = 1µA, 15 pF Load
PROGRAMMABLE, REDUCED SWING OUTPUT (ADAPTABLE TO CUSTOMERS REQUIREMENT)						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (VOL/VOH), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	ULPPO does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 2 for acceptable swing options V_{DD}: 1.5V – 3.63V, 10 pF Load, IOH / IOL = ±0.2 µA.
DC-Biased Programmable Output Voltage High Range	VOH		0.6 to 1.225		V	V_{DD}: 1.5V – 3.63V. IOH = -0.2 µA, 10 pF Load. See table 1 for acceptable VOH/VOL setting levels.
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	V_{DD}: 1.5V – 3.63V. IOL = 0.2 µA, 10 pF Load. See table 1 for acceptable VOH/VOL setting levels.
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, V_{DD} = 1.5V to 3.63V.

PIN DESCRIPTION

Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground. The GND pins can be connected together, as long as both GND pins are connected ground.
2	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The ULPPO oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
3	V_{DD}	Power Supply	Connect to power supply 1.5V ≤ V_{DD} ≤ 3.63V. Under normal operating conditions, V_{DD} does not require external bypass decoupling capacitor(s). For more information about the internal power-supply filtering, see Power-Supply Noise Immunity section in the detailed description. Contact PETERMANN-TECHNIK for applications that require a wider operating supply voltage range.

FIGURE 1. 1.5X0.8 MM PACKAGE (TOP VIEW)



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DESCRIPTION

The ULPPO is an ultra-small and ultra-low power 32.768 kHz high-precision oscillator optimized for battery-powered applications. The silicon oscillator technology enables a 32.768 kHz high-precision oscillator in the smallest footprint of 1.5x0.8mm housing. Typical core supply current is only 1 µA. And unlike standard oscillators, the ULPPO features programmable output swing, a factory programmable output that reduces the voltage swing to minimize power.

HIGH-PRECISION FREQUENCY STABILITY

The ULPPO is factory calibrated over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C² temperature coefficient, the ULPPO temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32.768 kHz ULPPO with extremely tight frequency stability over the -40°C to +85°C temperature range. Contact Petermann-Technik's engineers for applications that require a wider supply voltage range>3.63V, or lower operating frequency below 32.768 kHz.

When measuring the ULPPO output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32.768 kHz clock will give false readings with faster gate times.

POWER SUPPLY NOISE IMMUNITY

In addition to eliminating external output load capacitors common with standard XTALs, the ULPPO includes special power supply filtering and thus, eliminates the need for an external V_{DD} bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than ±150 mV noise and frequency components from low frequency to more than 10 MHz.

START-UP AND STEADY-STATE SUPPLY CURRENT

The ULPPO starts-up to a valid output frequency within 300 ms (180 ms typ). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 - 20 ms (to within 90% of V_{DD}).

During initial power-up, the ULPPO power-cycles internal blocks as shown in the power-supply start-up and steady state plot in the typical operating curves section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28 µA as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

OUTPUT VOLTAGE

The ULPPO has two output voltage options. One option is a standard DC-coupled LVCMOS output swing. The second option is the programmable output swing reduced swing output and current. Output swing is customer specific and factory programmed between 200 mV and 800 mV. For DC-coupled applications, output VOH and VOL are individually factory programmed to the customers' requirement. VOH programming range is between 600 mV and 1.225V in 100 mV increments. Similarly, VOL programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2V VIH and a 0.6V VIL. Simply select ULPPO programmable output swing factory programming code to be "D14" and the correct output thresholds will match the downstream IC or MCU input requirements. Interface logic will vary by manufacturer and we recommend that you review the input voltage requirements for the input interface.

For DC-biased programmable output swing configuration, the minimum VOL is limited to 350mV and the maximum allowable swing (VOH - VOL) is 750mV. For example, 1.1V VOH and 400mV VOL is acceptable, but 1.2V VOH and 400 mV VOL is not acceptable. When the output is interfacing to an XTAL input that is internally AC-coupled, the ULPPO output can be factory programmed to match the input swing requirements. For example, if a IC or MCU input is internally AC-coupled and requires an 800mV swing, then simply choose the ULPPO programming code "AA8" in the part number. It is important to note that the ULPPO does not include internal AC-coupling capacitors. Please see the *Part Number Ordering* section at the end of the datasheet for more information about the part number ordering scheme.

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ULPPO PROGRAMMABLE OUTPUT SWING

Figure 2 shows a typical ULPPO output waveform (into a 10 pF load) when factory programmed for a 0.70V swing and DC bias (V_{OH}/V_{OL}) for 1.8V logic:

EXAMPLE:

+ Programmable output swing part number coding: D14. Example part number: ULPPO18-1508-5A-W-32.768kHz-T-D14
+ V_{OH} = 1.1V, V_{OL} = 0.4V (V_{SW} = 0.70V)

FIGURE 2. ULPPO OUTPUT WAVEFORM (10 PF LOAD)

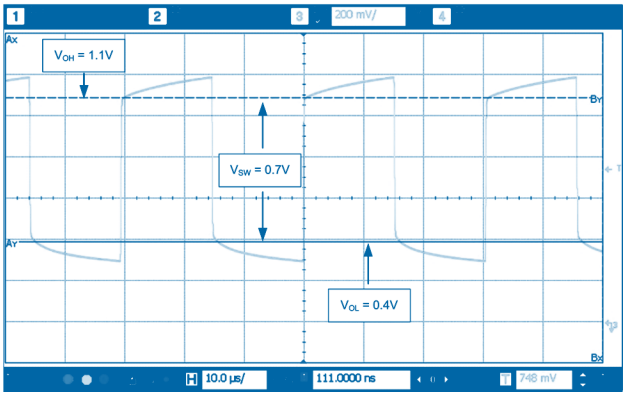


Table 1 shows the supported programmable output swing V_{OH}, V_{OL} factory programming options.

TABLE 1. ACCEPTABLE V_{OH}/V_{OL} PROGRAMMABLE OUTPUT SWING LEVELS

	V_{OH}(V)	V_{OL}(V)	SWING (mW)	COMMENTS
D26	1.2	0.6	600 ±55	1.8V logic compatible
D14	1.1	0.4	700 ±55	1.8V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

The values listed in Table 1 are nominal values at 25°C and will exhibit a tolerance of ±55 mV across V_{DD} and -40°C to 85°C operating temperature range.

ULPPO FULL SWING LVCMOS OUTPUT (STANDARD VERSION)

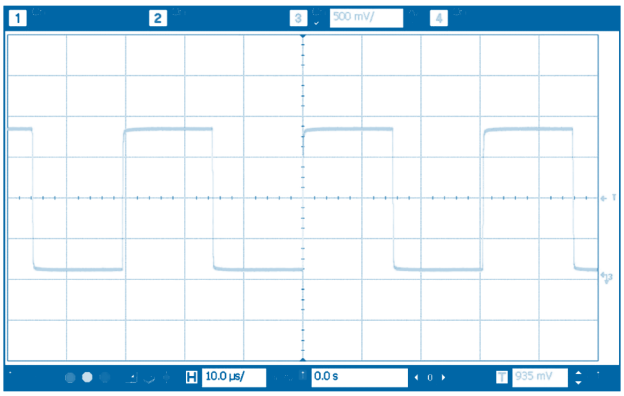
The ULPPO can be factory programmed to generate full-swing LVCMOS levels. Figure 3 shows the typical waveform (V_{DD} = 1.8V) at room temperature into a 15 pF load.

EXAMPLE:

+LVCMOS output part number coding is always S

+Example part number: ULPPO33-1508-5A-W-32.768KHZ-T-S

FIGURE 3. LVCMOS WAVEFORM (V_{DD} = 1.8V) INTO 15 PF LOAD



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CALCULATING LOAD CURRENT

NO LOAD SUPPLY CURRENT

When calculating no-load power for the ULPPO the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = I_{DD} Core + I_{DD} Output Driver

EXAMPLE 1: FULL-SWING LVCMOS

+ V_{DD} = 1.8V
+ I_{DD} Core = 990nA (typ)
+ $Vout_{pp}$ = 1.8V (LVCMOS)
+ I_{DD} Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA

Supply Current = 990nA + 206nA = 1.2µA

EXAMPLE 2: PROGRAMMED REDUCED SWING

+ V_{DD} = 1.8V
+ I_{DD} Core = 990nA (typ)
+ $Vout_{pp}$ (D14) = VOH – VOL = 1.1V - 0.4V = 700 mV
+ I_{DD} Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.7V)(32768Hz) = 80nA

TOTAL SUPPLY CURRENT WITH LOAD

To calculate the total supply current, including the load, follow the equation listed below. Note the 30% reduction in power with Programmable output swing.

Total Current = I_{DD} Core + I_{DD} Output Driver + Load Current

EXAMPLE 1: FULL-SWING LVCMOS

+ V_{DD} = 1.8V
+ I_{DD} Core = 990nA
+ Load Capacitance = 10pF
+ I_{DD} Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA
+ Load Current: (10pF)(1.8V)(32768Hz) = 590nA
+ Total Current = 990nA + 206nA + 590nA = 1.79µA

EXAMPLE 2: PROGRAMMED REDUCED SWING

+ V_{DD}= 1.8V
+ I_{DD} Core = 990nA
+ Load Capacitance = 10pF
+ $Vout_{pp}$ (Programmable): VOH – VOL = 1.1V - 0.4V = 700mV
+ I_{DD} Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.7V)(32768Hz) = 80nA
+ Load Current: (10pF)(0.5V)(32768Hz) = 229nA
+ Total Current = 990nA + 80nA + 229nA = 1.299µA

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TYPICAL OPERATING CURVES

FIGURE 4. FREQUENCY STABILITY OVER TEMPERATURE (PRE-REFLOW)

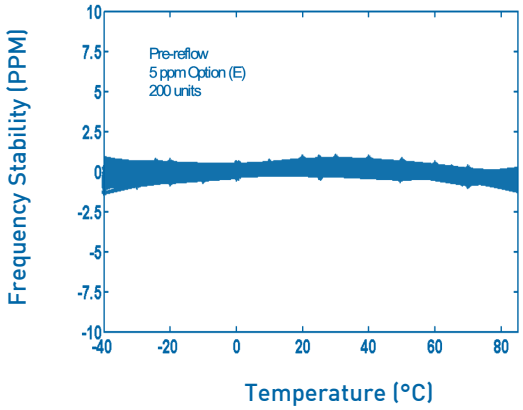


FIGURE 5. FREQUENCY STABILITY OVER TEMPERATURE (POST-REFLOW)

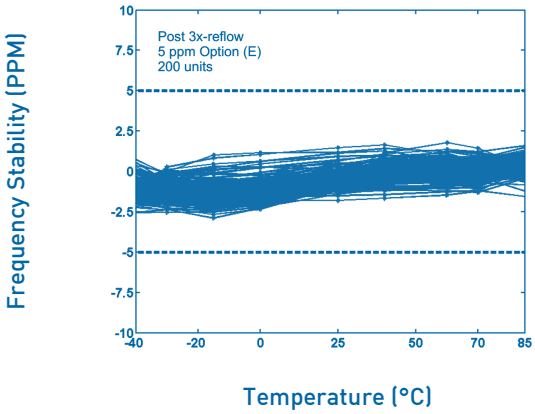


FIGURE 6. CORE CURRENT OVER TEMPERATURE

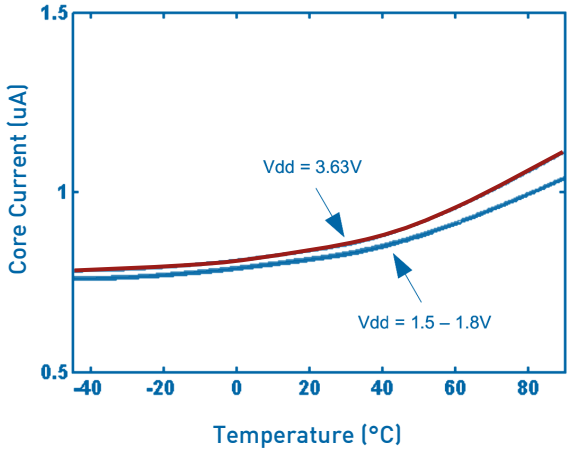


FIGURE 7. OUTPUT STAGE CURRENT OVER TEMPERATURE

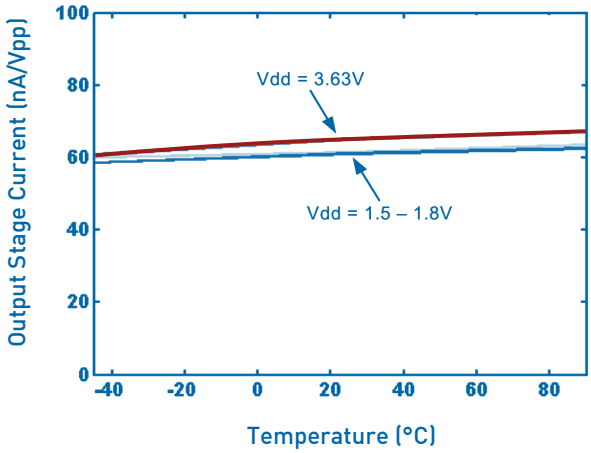


FIGURE 8. SUPPLY CURRENT OVER TEMPERATURE, LVCMOS (CORE + LVCMOS OUTPUT DRIVER, NO LOAD)

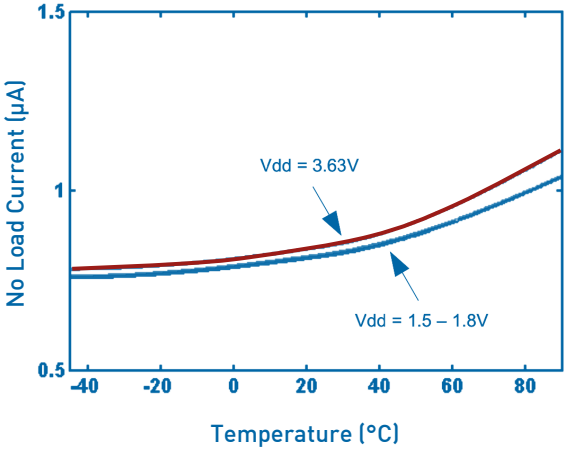
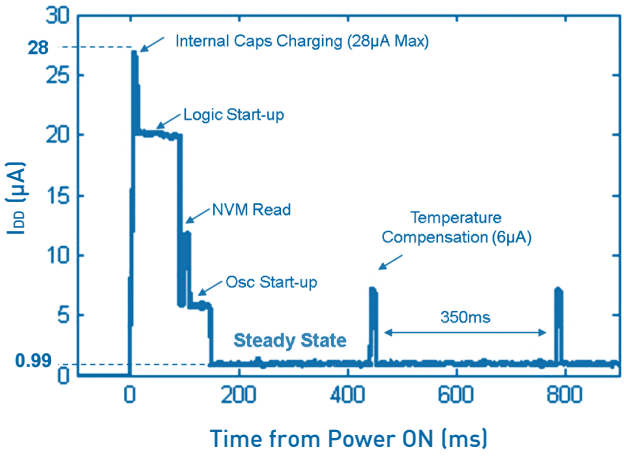


FIGURE 9. START-UP AND STEADY-STATE CURRENT PROFILE



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TYPICAL OPERATING CURVES

FIGURE 10. POWER SUPPLY NOISE REJECTION (+/-150mV NOISE)

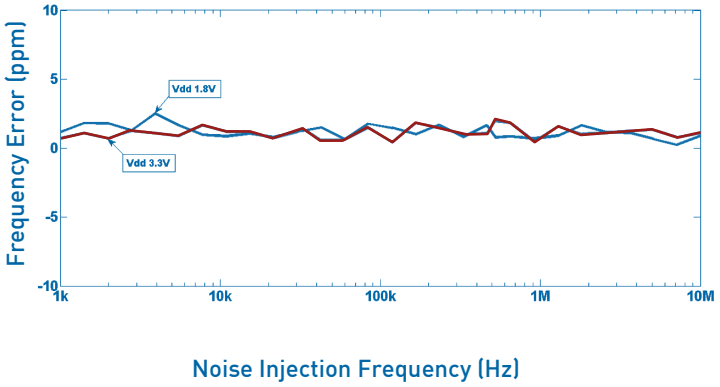


FIGURE 11. TEMPERATURE RAMP RESPONSE

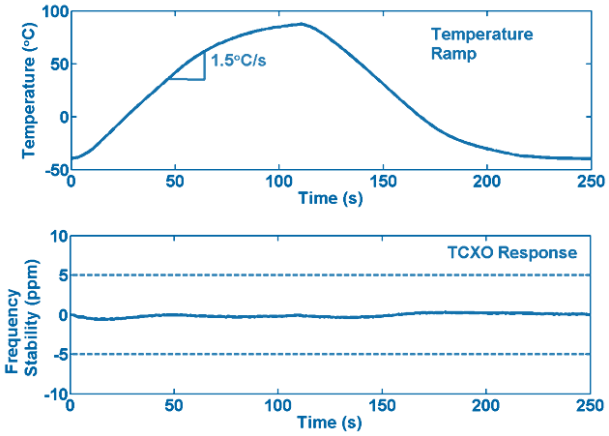


FIGURE 12. PROGRAMMABLE OUTPUT SWING WAVEFORM (V_{OH} = 1.1V, V_{OL} = 0.4V, 10 PF LOAD; ULPPO)

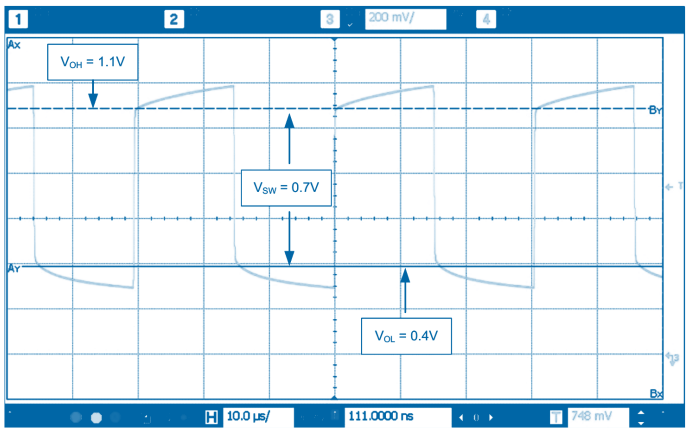
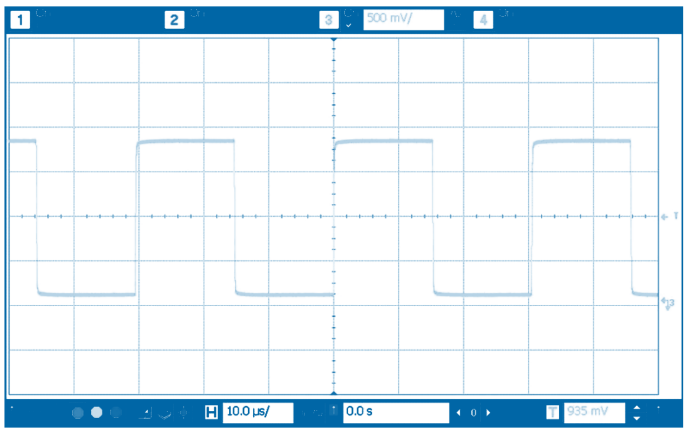


FIGURE 13. LVCMOS OUTPUT WAVEFORM (V_{SWING} = 1.8V, ULPPO,10 PF LOAD)



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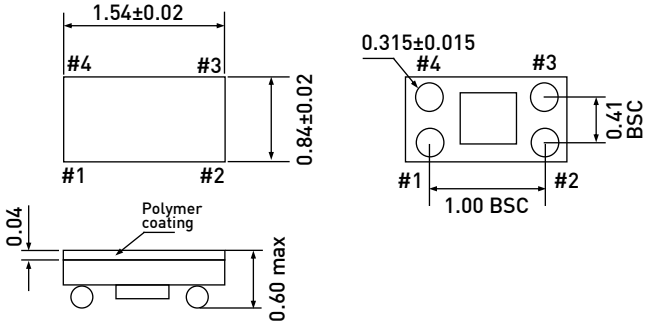
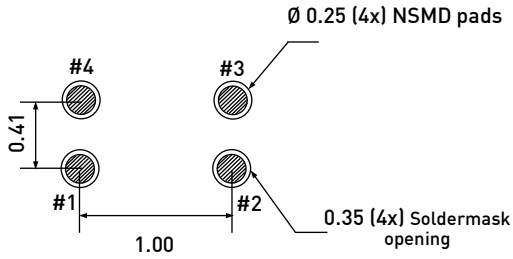
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

1.55 X 0.85 MM



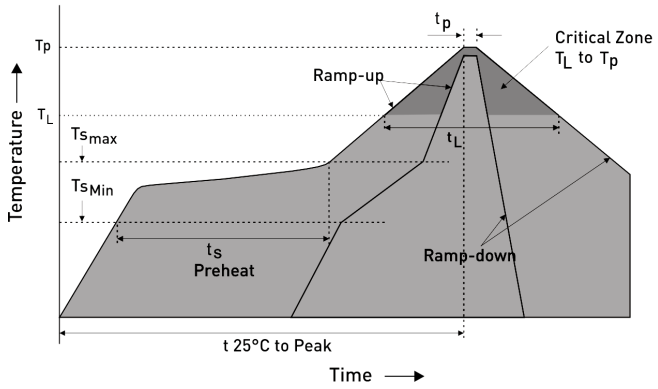
RECOMMENDED LAND PATTERN (UNIT:MM)



(soldermask openings shown with heavy dashed line)

Recommended 4-mil (0.1mm) stencil thickness

REFLOW SOLDER PROFILE



IPC/JEDEC Standard	IPC/JEDEC J-STD-020
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Typical (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum
Target Peak Temperature (TP Target)	255°C
Time within 5°C of actual peak (tP)	20 -40 Seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

MANUFACTURING GUIDELINES:

1. No Ultrasonic Cleaning: Do not subject the ULPPO to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the structure may occur.
2. Do not apply underfill to the ULPPO. The device will not meet the frequency stability specification if underfill is applied.
3. Reflow profile, per JESD22-A113D.

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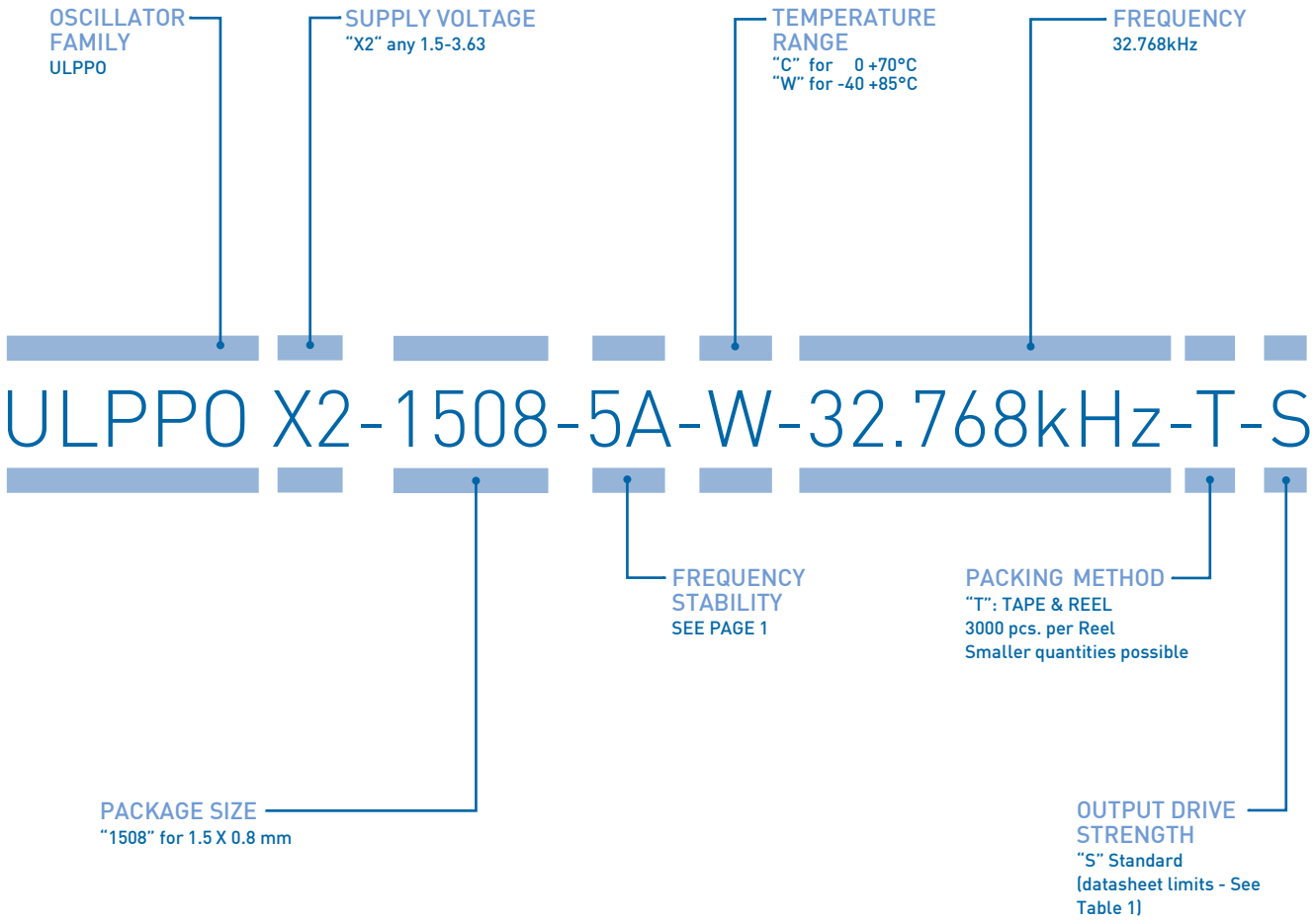
ORDERING INFORMATION



EXAMPLE: ULPPOX2-1508-5A-W-32.768kHz-T-S

PLEASE CLICK HERE TO CREATE YOUR OWN ORDERING CODE

EXPRESS SAMPLES ARE DELIVERABLE ON THE SAME DAY IF ORDERED UNTIL 02:00 PM!

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REVISION HISTORY[4]

VERSION	RELEASE DATE	AMENDMENTS SUMMARY
01	10/18/2016	+ Added 5pF LVCMOS rise/fall time spec. + Updated Programmable, Reduced Swing Output section + Updated first year aging spec. condition + Added 10-year and 20-year aging spec. + Added Manufacturing Guidelines

Note:

4. Based on Datasheet version from November 2014/SPEC 01/REV.00

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PREMIUM QUALITY BY PETERMANN-TECHNIK

DMSZ
certified according to
ISO 9001
QM 00886

OUR COMPANY IS CERTIFIED ACCORDING TO ISO 9001:2015 IN OCTOBER 2016 BY THE DMSZ CERTIFIKATION GMBH.

THIS IS FOR YOU TO ENSURE THAT THE PRINCIPLES OF QUALITY MANAGEMENT ARE FULLY IMPLEMENTED IN OUR QUALITY MANAGEMENT SYSTEM AND QUALITY CONTROL METHODS ALSO DOMINATE OUR QUALITY STANDARDS.